AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0001] as follows:

[0001] This application is related to co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,973 entitled "MULTILEVEL CACHE STRUCTURE AND METHOD USING MULTIPLE ISSUE ALGORITHM WITH OVER SUBSCRIPTION AVOIDANCE FOR HIGH BANDWIDTH CACHE PIPELINE" filed February 21, 2000, now issued as U.S. Patent No. 6,427,189, co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,283 entitled "CACHE CHAIN STRUCTURE TO IMPLEMENT HIGH BANDWIDTH LOW LATENCY CACHE MEMORY SUBSYSTEM" filed February 21, 2000, now issued as U.S. Patent No. 6,557,078, co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,285 entitled "L1 CACHE MEMORY" filed February 21, 2000, now issued as U.S. Patent No. 6,507,892, co-pending and commonly assigned U.S. Patent Application Serial Number 09/501,396 entitled "METHOD AND SYSTEM FOR EARLY TAG ACCESSES FOR LOWER-LEVEL CACHES IN PARALLEL WITH FIRST-LEVEL CACHE" filed February 9, 2000, now issued as U.S. Patent No. 6,427,188, co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,279 entitled "CACHE ADDRESS CONFLICT MECHANISM WITHOUT STORE BUFFERS" filed February 21, 2000, now issued as U.S. Patent No. 6,539,457, co-pending and commonly assigned U.S. Patent Application Serial Number 09/507,546 entitled "SYSTEM AND METHOD UTILIZING SPECULATIVE CACHE ACCESS FOR IMPROVED PERFORMANCE" filed February 18, 2000, now issued as U.S. Patent No. 6,647,464, and co-pending and commonly assigned U.S. Patent Application Serial Number 09/507,241 entitled "METHOD AND SYSTEM FOR PROVIDING A HIGH BANDWIDTH CACHE THAT ENABLES SIMULTANEOUS READS AND WRITES WITHIN THE CACHE" filed February 18, 2000 (now abandoned), the disclosures of which are hereby incorporated herein by reference.

Please amend paragraph [0031] as follows:

[0031] More recently, a more efficient cache architecture that does not require such progression through the various levels of cache in a serial fashion has been developed, such as is disclosed in co-pending and commonly assigned U.S. Patent Application Serial Number 09/501,396 entitled "METHOD AND SYSTEM FOR EARLY TAG ACCESSES FOR

LOWER-LEVEL CACHES IN PARALLEL WITH FIRST-LEVEL CACHE" filed February 9, 2000, now issued as U.S. Patent No. 6,427,188, and co-pending and commonly assigned U.S. Patent Application Serial Number 09/507,546 entitled "SYSTEM AND METHOD UTILIZING SPECULATIVE CACHE ACCESS FOR IMPROVED PERFORMANCE" filed February 18, 2000, now issued as U.S. Patent No. 6,647,464. It will be appreciated that embodiments of the present invention may be implemented within, as examples, a cache structure such as that of Fig. 1, or within more efficient cache structures such as those disclosed in co-pending U.S. Patent Applications "METHOD AND SYSTEM FOR EARLY TAG ACCESSES FOR LOWER-LEVEL CACHES IN PARALLEL WITH FIRST-LEVEL CACHE" and "SYSTEM AND METHOD UTILIZING SPECULATIVE CACHE ACCESS FOR IMPROVED PERFORMANCE."

Please amend paragraph [0036] as follows:

[0036] For greater efficiency, the cache architecture is preferably implemented to enable levels thereof to be speculatively accessed as disclosed in co-pending and commonly assigned U.S. Patent Application Serial Number 09/501,396 entitled "METHOD AND SYSTEM FOR EARLY TAG ACCESSES FOR LOWER-LEVEL CACHES IN PARALLEL WITH FIRST-LEVEL CACHE" filed February 9, 2000, now issued as U.S. Patent No. 6,427,188, and co-pending and commonly assigned U.S. Patent Application Serial Number 09/507,546 entitled "SYSTEM AND METHOD UTILIZING SPECULATIVE CACHE ACCESS FOR IMPROVED PERFORMANCE" filed February 18, 2000, now issued as U.S. Patent No. 6,647,464. It should be understood, however, that embodiments of the present invention may be implemented in any suitable cache structure of the prior art, including cache structures that do not provide for speculative accessing of cache levels. Also, as further described hereafter, a preferred embodiment of the present invention enables out-of-order processing of access requests in the pending request queue.

Please amend paragraph [0040] as follows:

[0040] In one implementation of a preferred embodiment, bits [14:8] of the physical address may be decoded to identify any of the 128 indexes of a bank. Also, in one implementation of a preferred embodiment, bits [7:4] of the physical address are decoded to select to which bank an access is to be issued, as is disclosed in greater detail in co-pending

and commonly assigned U.S. Patent Application Serial Number 09/507,546 entitled "SYSTEM AND METHOD UTILIZING SPECULATIVE CACHE ACCESS FOR IMPROVED PERFORMANCE" filed February 18, 2000, now issued as U.S. Patent No. 6,647,464. Of course, in various alternative implementations different bits may be utilized for identifying a bank for an access request, and any such implementation is intended to be within the scope of the present invention.

Please amend paragraph [0044] as follows:

[0044] A preferred embodiment provides a system and method for determining/recognizing such bank conflicts and resolving them in a manner that enables efficient utilization of the cache. Of course, conflicts other than those described above may be encountered, and the cache architecture of a preferred embodiment may further be implemented to enable efficient recognition and resolution of any such conflicts. For example, "over subscription" (e.g., over subscription of integer resources and/or over subscription of floating point resources) is another type of conflict that may be encountered within the cache architecture. To enable efficient resolution/avoidance of such over subscription, a preferred embodiment may be implemented as disclosed in co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,973 entitled "MULTILEVEL CACHE STRUCTURE AND METHOD USING MULTIPLE ISSUE ALGORITHM WITH OVER SUBSCRIPTION AVOIDANCE FOR HIGH BANDWIDTH CACHE PIPELINE" filed February 21, 2000, now issued as U.S. Patent No. 6,427,189.

Please amend paragraph [0052] as follows:

[0052] Preferably, the pending request queue for a level of cache is implemented with the capability of issuing pending access requests out of order. For instance, in contrast to the example shown in Fig. 2A, a preferred embodiment is implemented with the capability to issue requests A, E, F, and G in clock cycle 1, assuming that such requests are not otherwise conflicted. Thus, conflicts between older requests (e.g., between requests A-D of Fig. 2A) does not necessarily delay the issuance of non-conflicted newer requests (e.g., requests E-H of Fig. 2A). Examples of such out-of-order processing are further disclosed in co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,973 entitled "MULTILEVEL CACHE STRUCTURE AND METHOD USING MULTIPLE

ISSUE ALGORITHM WITH OVER SUBSCRIPTION AVOIDANCE FOR HIGH BANDWIDTH CACHE PIPELINE" filed February 21, 2000, now issued as U.S. Patent No. 6,427,189, co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,283 entitled "CACHE CHAIN STRUCTURE TO IMPLEMENT HIGH BANDWIDTH LOW LATENCY CACHE MEMORY SUBSYSTEM" filed February 21, 2000, now issued as U.S. Patent No. 6,557,078, and co-pending and commonly assigned U.S. Patent Application Serial Number 09/510,285 entitled "L1 CACHE MEMORY" filed February 21, 2000, now issued as U.S. Patent No. 6,507,892.